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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,580	01/23/2001	John F. McMahon	42390.P5142D	3565

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,580	MCMAHON, JOHN F.	
	Examiner	Art Unit	
	Alonzo Chambliss	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/5/04 has been entered.

Response to Arguments

2. Applicant's arguments filed 4/5/04 have been fully considered but they are not persuasive.

In regards to Templeton can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. First, Templeton is not combined with another reference. Second, it would have been obvious to one having ordinary skill in the art at the time the invention was made to flip the substrate so that the side that does not have the flip-chip mounted to it is mounted to the plurality of shelves, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse, 86 USPQ 70.* Therefore, it would have been obvious to rearrange the substrate of Templeton so that the side that does not have the flip-chip mounted to it is mounted to the plurality of shelves, since by flipping the substrate the flip chip can be electrically connected to the

plurality of shelves without the use of a via, which would shorter the electrical distance between devices.

In regards to the via not being eliminated between the devices. The via would not be need since once the substrate is flipped, trace 304 would simply extend directly to electrically conductive material 309 thus the via 306 and trace 307 would not be need to make the electrical connection between the devices. Furthermore, the device of Templeton can function with the chip in or outside of the cavity without hindering the performance of the semiconductor device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 28, 29, 31-33, and 35-40-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Templeton, Jr. et al. (U.S. 5,874,321).

With respect to Claim 28, Templeton discloses electrically connecting a semiconductor die 704 to at least one of a plurality of shelves 702-1 - 702-N, electrically connecting a flip-chip 7033-703c to a ceramic substrate 706, and attaching the ceramic substrate 706 to one of the plurality of shelves 702-1 -702-N (see col. 9 lines 44-67 and col. 10 lines 1-58*, Fig. 7). Templeton does not explicitly disclose that the substrate side that does not have the flip-chip mounted to it is mounted to the plurality of shelves.

However, one skilled in the art at the time of the invention would have readily recognize flip the substrate so that the side that does not have the flip-chip mounted to it is mounted to the plurality of shelves, since by flipping the substrate the flip chip can be electrically connected to the plurality of shelves without the use of a via, which would shorter the electrical distance between devices. Therefore, it would have been obvious to rearrange the substrate of Templeton so that the side that does not have the flip-chip mounted to it is mounted to the plurality of shelves with the process of Templeton, since by flipping the substrate the flip chip can be electrically connected to the plurality of shelves without the use of a via, which would shorter the electrical distance between devices.

With respect to Claim 29, Templeton discloses electrically connecting the ceramic substrate 706 to at least one of the plurality of shelves 702-1 - 702-N (see Fig. 7).

With respect to Claim 31, Templeton discloses wherein attaching the ceramic substrate 706 to one of the plurality of shelves 702-1 -702-N provides a lid above the semiconductor die 704 (see Fig. 7).

With respect to Claim 32, Templeton discloses electrically testing the electrically connected flip-chip 703a-703c before attaching of the ceramic substrate 706 to one of the plurality of shelves 702-1 - 702-N (see col. 10 lines 59-65).

With respect to Claim 33, Templeton discloses wherein electrically connecting the flip-chip 703a to the ceramic substrate 706 comprises electrically connecting the flip-chip 703a to the ceramic substrate 706 with solder balls (see col. 10 lines 3-10).

With respect to Claim 34, Templeton discloses disposing a seal 712 between a base of the ceramic substrate 706 and one of said plurality of shelves (i.e. 702C) to which the ceramic substrate 706 is attached (see Fig. 7).

With respect to Claims 36 and 37, Templeton discloses wherein electrically connecting the semiconductor die 301 to the at least one of a plurality of shelves comprises electrically connecting a CPU chip to the at least one of the plurality of shelves. Also, wherein electrically connecting the flip-chip 308 to the ceramic substrate 302 comprises electrically connecting a memory cache (i.e. Memory chips) flip-chip 308 to the ceramic 302 (see col. 5 lines 61-67', Figs.3A and 4).

With respect to Claim 38, Templeton discloses wherein electrically connecting the semiconductor die 704 to at least one of the plurality of shelves 702-1 - 702-N comprises electrically connecting the semiconductor die 704 to the at least one of a plurality of shelves 702-1 - 702-N with at least one bond wire (see col. 10 lines 3-10).

With respect to Claims 39 and 40, Templeton discloses including attaching the semiconductor die 301 to a heat slug 305 (i.e. heat sink), wherein the heat slug 305 is attached to at least one of a plurality of shelves (see col. 5 lines 4-15 and 38-44, Fig. 3A).

5. Claims 30 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Templeton, Jr. et al. (U.S. 5,874,321) as applied to claim 28 above, and further in view of Gaudenzi et al. (U.S. 5,313,366).

With respect to Claim 30, Templeton fails to disclose wherein electrically connecting the ceramic substrate to at least one of said plurality of shelves comprises

electrically connecting the ceramic substrate to at least one of the plurality of shelves with at least one bond wire. However, Gaudenzi discloses wherein electrically connecting the ceramic substrate (i.e. chip carrier) 150 to at least one of the plurality of shelves comprises electrically connecting the ceramic substrate 150 to at least one of the plurality of shelves with at least one bond wire 152 (see col. 3 lines 46-61 and col. 4 lines 50-64;Fig. 4B). Therefore, it would have been obvious to incorporate wire bonding the substrate to a plurality of shelves with the process of Templeton, since the wire bonding would facilitate a direct electrical connection between the substrate (i.e. chip carrier) with the plurality of shelves as taught by Gaudenzi.

With respect to Claim 34, Gaudenzi discloses covering the flip chip 106 with an encapsulant 142 (see col. 4 lines 24-35;Fig. 3B).

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

6. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

Alonzo Chambliss
Primary Patent Examiner
Art Unit 2827

AC/April 16, 2004